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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,996	12/10/2003	Ji-Young Kim	259/024	6742

27849 7590 03/10/2006

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EXAMINER	
NGUYEN, CUONG QUANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,996	KIM ET AL.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-63 is/are pending in the application.

4a) Of the above claim(s) 15-63 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12-10-03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election of Group I, claims 1-14 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims are rejected under 35 U.S.C. 102(b) as being anticipated by Adkisson et al. (US 6,448,590).

Regarding claims 1, 6, Adisson et al. discloses a self-aligned inner gate recess channel in a semiconductor substrate, comprising: a recess trench (52) formed in an active region of the substrate; a gate dielectric layer (an oxide layer 61) formed on a bottom portion of the recess trench; recess inner nitride sidewall spacers (78) formed on sidewalls of the recess trench; a gate formed in the recess trench so that an upper

portion (top portion of layer 68) of the gate protrudes above an upper surface of the substrate, wherein a thickness of the recess inner sidewall spacers causes a center portion of the gate to have a smaller width than the protruding upper portion and a lower portion (layer 60) of the gate; a gate mask (layer 74) formed on the gate layer; gate sidewall spacers (layer 72) formed on the protruding upper portion of gate and on (bottom surface of) the gate mask; and a source/drain region (46) formed in the active region of the substrate adjacent the gate sidewall spacers. See Adkisson et al.'s Fig.9-11.

Regarding claim 9, it is noted that nitride spacer is known in a art as a silicon nitride spacer.

Regarding claims 10, 11, as shown in Ahkisson et al.'s Fig.9-11, the gate formed in the recess trench comprises: a first gate layer (a polysilicon layer 62) (col.6 lines 65-67) formed in a bottom portion of the recess trench; and a second gate layer (66) formed on the first gate layer in an upper portion of the recess trench, the second gate layer having a lower portion within the recess trench and an upper portion that protrudes above the upper surface of the substrate, wherein a thickness of the recess inner sidewall spacers causes the lower portion of the second gate layer to have a smaller width than the protruding upper portion of the second gate layer and the first gate layer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6, and 9-11are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda et al. (US 5,371,024) in view of Tung (US 6,150,219).

Regarding claims 1, 14, Hieda et al. discloses a self-aligned inner gate recess channel in a semiconductor substrate, comprising: a recess trench formed in an active region of the substrate; a gate dielectric layer (9) formed on a bottom portion of the recess trench; a gate (10) formed in the recess trench so that an upper portion (top portion of layer 10) of the gate protrudes above an upper surface of the substrate; a gate mask (a portion of insulating layer 13 directly on top surface of the protruded portion of the gate) formed on the gate layer; gate sidewall spacers (a portion of insulating layer cover side surfaces of the protruded portion of the gate) formed on the protruding upper portion of gate and on the gate mask; and a source/drain region (an n^+ region 12)

formed in the active region of the substrate adjacent the gate dielectric layer on the sidewall of the trench. See Hieda et al.'s Fig.3B-3D.

Hieda et al. does not teach that recess inner sidewall spacers formed on sidewalls of the recess trench.

Tung at al. discloses a self-aligned inner gate recess channel in a semiconductor substrate, comprising: recess inner sidewall spacers (230) formed on sidewalls of the recess trench, wherein a thickness of the recess inner sidewall spacers causes a center portion of a gate (250) to have a smaller width than un upper portion and a lower portion of the gate. See Tung's Fig.2G.

It would have been obvious to one of ordinary skill in the art to incorporate the recess inner sidewall as taught by Tung into Hieda et al.'s device in order to reduce the effect of the high bias on the trench gate. See Tung's col.4 lines 65-67.

It is noted that the limitations "a recess trench formed in an active region of the substrate, wherein a thickness of the recess inner sidewall spacers causes a center portion of the gate to have a smaller width than the protruding upper portion and a lower portion (layer 60) of the gate" and "a source/drain region formed in the active region of the substrate adjacent the gate sidewall spacers" would flow naturally in the combination of Hieda et al. and Tung.

Regarding claim 9, Tung teach that the recess inner sidewall is a field oxide layer which is known in the art as silicon oxide layer.

Regading claims 10, 11 and 13, Hieda et al. teach that the gate (10) is formed of polisicon (col.4 lines 5-10), so the bottom portion of layer (10) is considered as a first gate layer and an upper portion of layer (10) is considered as a second gate layer.

Claims 2, 3, 7, 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adkisson et al.

Adkisson et al. teaches all the linitations of claims 1, 6, and 9-11 but does not explicitly teach the dimensions of the trench opening (claim 2), the trench depth (claim 3), the thickess of the gate dielectric (claim 7), the thickness of the recess inner sidewall (claim 8), the thickness of the first gate layer (claim 12).

It would have bben obvious to one of ordinary skill in the art to provide above dimensions as claimed in claims 2, 3, 7, 8 and 12 because these dimensions would have been determinable by one of ordinary skill in the art through no more than routine experimentation. See In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda et al. in view of (US 6,150,219) and further in view of Farrar (US 6,677,209).

Regarding claim 4, Hieda et al. further teaches that the substrate comprises an isolation region (locos region 3); the active region includes a well region (col.3 lines 60-65), source/drain region 912) and a threshold voltage control region (8). However, Hieda et al. does not teach that the isolation region is a STI region.

Farrar teaches that STI and LOCOS region are commonly used for definind the active region and they are interchangeable. See Farrar's col.20-26.

It would have been obvious to one of ordinary skill in the art to use STI structure instead of LOCOS structure as taught by Farrar into Hieda et al.'s device in order to eliminate the birds beak of LOCOS and to provide a high degree of surface planarity. See Farrar's col.2 lines 26-29.

Regarding claim 5, Farrar does not teach that STI having a depth of approximately 3,000 angstroms.

It would have been obvious to one of ordinary skill in the art to provide the STI with a depth as claimed because the depth of STI structure would have been determinable by one of ordinary skill in the art through no more than routine experimentation. See In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Conclusion

4. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (571) 273-8300. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

5. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (571) 272-1661. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Eddie Lee who can be reached on (571) 272-1732.

Cuong Nguyen

Primary examiner

3/3/06